

AMENDMENTS TO THE CLAIMS

Please amend claims 36, 49, 62, 63, 71, 73 and 74 as follows:

Claims 1 – 35 (Cancelled)

36. (Currently Amended) A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using $\text{Ga}_v\text{Al}_{1-v}$ $\text{Ga}_v\text{Al}_{1-v}$, (where, $0 \leq v \leq 1$) as a main component of [[the]] Group III-elements and N as a main component of [[the]] Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer, and a third layer is in contact with said second layer;

said second metal layer comprises a metal material having a higher melting point than those of the metal materials in said first metal layer and said third metal layer;

said third metal layer comprises a metal material having a lower resistivity than those of the metal materials in said first metal layer and said second metal layer;

said first metal layer comprises any metal material selected from a group comprising Ni, Pt, Pd, $\text{Ni}_z\text{Si}_{1-z}$, $\text{Pt}_z\text{Si}_{1-z}$, $\text{Pd}_z\text{Si}_{1-z}$, $\text{Ni}_z\text{N}_{1-z}$, and $\text{Pd}_z\text{N}_{1-z}$, (where, $0 < z < 1$); and

said second metal layer comprises any metal material selected from a group comprising Mo, W, Ta, $\text{Mo}_x\text{Si}_{1-x}$, $\text{Pt}_x\text{Si}_{1-x}$, $\text{W}_x\text{Si}_{1-x}$, $\text{Ti}_x\text{Si}_{1-x}$, $\text{Ta}_x\text{Si}_{1-x}$, $\text{Mo}_x\text{N}_{1-x}$, $\text{Mo}_{1-x}\text{N}_x$, W_xN_{1-x} , $\text{Ti}_x\text{N}_{1-x}$, and $\text{Ta}_x\text{N}_{1-x}$, (where, $0 < x < 1$).

37. (Previously Presented) The semiconductor device according to claim 36, wherein said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

38. (Previously Presented) The semiconductor device according to claim 36, wherein said first metal material comprises a metal material having a higher work function than that of the metal material in said second metal material.

39. (Previously Presented) The semiconductor device according to claim 38, wherein said metal layer comprises a metal material having a higher work function than that of the metal material in said third metal layer.

40. (Previously Presented) The semiconductor device according to claim 36, wherein the melting point of said second metal layer is 1,000°C or higher.

41. (Previously Presented) The semiconductor device according to claim 36, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

42. (Previously Presented) The semiconductor device according to claim 41, wherein said substrate comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate, and a GaN substrate.

43. (Previously Presented) The semiconductor device according to claim 36, wherein said semiconductor layer is an $\text{Al}_u\text{Ga}_{1-u}\text{N}$ layer (where, $0 \leq u \leq 1$).

44. (Previously Presented) The semiconductor device according to claim 36, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

45. (Previously Presented) The semiconductor device according to claim 44, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and a GaN compound semiconductor electron supplying layer comprises AlGaN.

46. (Previously Presented) The semiconductor device according to claim 36, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

47. (Previously Presented) The semiconductor device according to claim 46, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

48. (Previously Presented) The semiconductor device according to claim 36, wherein said semiconductor layer is a n-type GaN channel layer.

49. (Currently Amended) A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using $\text{Ga}_v\text{Al}_{1-v}$ (where, $0 \leq v \leq 1$) as a main component of [[the]] Group III-elements and N as a main component of [[the]] Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer, and a third layer is in contact with said second layer;

said second metal layer comprises a metal material having a higher melting point than those of the metal materials in said first metal layer and said third metal layer;

said third metal layer comprises a metal material having a lower resistivity than those of the metal materials in said first metal layer and said second metal layer;

said first metal layer comprises any metal material selected from a group comprising $\text{Ni}_{z1}\text{Si}_{l-z1}$ (where, $0.4 \leq z1 \leq 0.75$), $\text{Pt}_{z2}\text{Si}_{l-z2}$ (where, $0.5 \leq z2 \leq 0.75$), $\text{Pd}_{z3}\text{Si}_{l-z3}$ (where, $0.5 \leq z3 \leq 0.85$), $\text{Ni}_{z4}\text{N}_{1-z4}$ (where, $0.5 \leq z4 \leq 0.85$), and $\text{Pd}_{z5}\text{N}_{1-z5}$ (where, $0.5 \leq z5 \leq 0.85$); and

said second metal layer comprises any metal material selected from a group comprising Mo, W, Ta, $\text{Mo}_x\text{Si}_{l-x}$, $\text{Pt}_x\text{Si}_{l-x}$, $\text{W}_x\text{Si}_{l-x}$, $\text{Ti}_x\text{Si}_{l-x}$, $\text{Ta}_x\text{Si}_{l-x}$, $\text{Mo}_x\text{N}_{1-x}$, W_xN_{1-x} , $\text{Ti}_x\text{N}_{1-x}$, and $\text{Ta}_x\text{N}_{1-x}$, (where, $0 < x < 1$).

50. (Previously Presented) The semiconductor device according to claim 49, wherein said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

51. (Previously Presented) The semiconductor device according to claim 49, wherein said first metal layer comprises a metal material having a higher work function than that of the metal material in said second metal layer.

52. (Previously Presented) The semiconductor device according to claim 51, wherein said first metal layer comprises a metal material having a higher work function than that of the metal material in said third metal layer.

53. (Previously Presented) The semiconductor device according to claim 49, wherein the melting point of said second metal layer is 1,000°C or higher.

54. (Previously Presented) The semiconductor device according to claim 49, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

55. (Previously Presented) The semiconductor device according to claim 54, wherein said substrate comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate and a GaN substrate.

56. (Previously Presented) The semiconductor device according to claim 49, wherein said semiconductor layer is an $\text{Al}_u\text{Ga}_{1-u}\text{N}$ layer (where, $0 \leq u \leq 1$).

57. (Previously Presented) The semiconductor device according to claim 49, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

58. (Previously Presented) The semiconductor device according to claim 57, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and GaN compound semiconductor electron supplying layer comprises AlGaN.

59. (Previously Presented) The semiconductor device according to claim 49, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

60. (Previously Presented) The semiconductor device according to claim 59, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

61. (Previously Presented) The semiconductor device according to claim 49, wherein said semiconductor layer is a n-type GaN channel layer.

62. (Currently Amended) A semiconductor device comprising a semiconductor layer comprising a compound semiconductor using $\text{Ga}_v\text{Al}_{1-v}$ (where, $0 \leq v \leq 1$) as a main component of [[the]] Group III-elements and N as a main component of [[the]] Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher melting point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower resistivity than that of the metal material in said first metal layer; and

said first metal layer comprises any metal material selected from a group comprising $\text{Ni}_y\text{N}_{1-y}$ and $\text{Pd}_y\text{N}_{1-y}$ (where, $0 < y < 1$).

63. (Currently Amended) The semiconductor device according to claim 62 A semiconductor device comprising a semiconductor layer comprising a compound semiconductor using $\text{Ga}_v\text{Al}_{1-v}$ (where, $0 \leq v \leq 1$) as a main component of Group III-elements and N as a main component of Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher melting point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower resistivity than that of the metal material in said first metal layer: and

said first metal layer comprises any metal material selected from a group comprising $\text{Ni}_y\text{N}_{1-y}$ and $\text{Pd}_y\text{N}_{1-y}$ (where, $0 < y < 1$),

wherein said second metal layer comprises any metal material selected from a group comprising any metal material selected from a group comprising Au, Cu, Al, and Pt.

64. (Previously Presented) The semiconductor device according to claim 62, wherein said first metal layer has a higher work function than said second metal layer.

65. (Previously Presented) The semiconductor device according to claim 62, wherein the melting point of said first metal layer is 1,000°C or higher.

66. (Previously Presented) The semiconductor device according to claim 62, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

67. (Previously Presented) The semiconductor device according to claim 66, wherein said substrate comprises any substrate selected from a group a sapphire substrate, a SiC substrate, and a GaN substrate.

68. (Previously Presented) The semiconductor device according to claim 62, wherein said semiconductor layer is an $\text{Al}_u\text{Ga}_{1-u}\text{N}$ layer (where, $0 \leq u \leq 1$).

69. (Previously Presented) The semiconductor device according to claim 62, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

70. (Previously Presented) The semiconductor device according to claim 69, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and GaN compound semiconductor electron supplying layer comprises AlGaN.

71. (Currently Amended) ~~The semiconductor device according to claim 62 A~~
semiconductor device comprising a semiconductor layer comprising a compound
semiconductor using $\text{Ga}_v\text{Al}_{1-v}$ (where, $0 \leq v \leq 1$) as a main component of Group III-
elements and N as a main component of Group V-elements and a Schottky junction
metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure
wherein a first metal layer is in contact with said semiconductor layer and a second
metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher melting
point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower
resistivity than that of the metal material in said first metal layer; and

said first metal layer comprises any metal material selected from a group
comprising $\text{Ni}_y\text{N}_{1-y}$ and $\text{Pd}_y\text{N}_{1-y}$ (where, $0 < y < 1$),

wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

72. (Previously Presented) The semiconductor device according to claim 71, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

73. (Currently Amended) ~~The semiconductor device according to claim 62 A~~
semiconductor device comprising a semiconductor layer comprising a compound
semiconductor using $\text{Ga}_v\text{Al}_{1-v}$ (where, $0 \leq v \leq 1$) as a main component of Group III-
elements and N as a main component of Group V-elements and a Schottky junction
metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure
wherein a first metal layer is in contact with said semiconductor layer and a second
metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher melting point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower resistivity than that of the metal material in said first metal layer: and

said first metal layer comprises any metal material selected from a group comprising Ni_yN_{1-y} and Pd_yN_{1-y} (where, $0 < y < 1$),

wherein said semiconductor layer is a n-type GaN channel layer.

74. (Currently Amended) A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leq v \leq 1$) as a main component of [[the]] Group III-elements and N as a main component of [[the]] Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher melting point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower resistivity than that of the metal material of said first metal layer: and

said first metal layer comprises any metal material selected from a group comprising $Ni_{y4}N_{1-y4}$ and $Pd_{y5}N_{1-y5}$ (where, $0.5 \leq y_5 \leq 0.85$ and $0.5 \leq y_4 \leq 0.85$).

75. (Previously Presented) The semiconductor device according to claim 74, wherein said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

76. (Previously Presented) The semiconductor device according to claim 74, wherein said first metal layer has a higher work function than said second metal layer.

77. (Previously Presented) The semiconductor device according to claim 74, wherein the melting point of said first metal layer is 1,000°C or higher.

78. (Previously Presented) The semiconductor device according to claim 74, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

79. (Previously Presented) The semiconductor device according to claim 78, wherein said substrate comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate, and a GaN substrate.

80. (Previously Presented) The semiconductor device according to claim 74, wherein said semiconductor layer is an $\text{Al}_u\text{Ga}_{1-u}\text{N}$ layer (where, $0 \leq u \leq 1$).

81. (Previously Presented) The semiconductor device according to claim 74, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

82. (Previously Presented) The semiconductor device according to claim 81, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

83. (Previously Presented) The semiconductor device according to claim 74, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

84. (Previously Presented) The semiconductor device according to claim 83, wherein said GaN semiconductor channel layer comprises a compound semiconductor selected from GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

85. (Previously Presented) The semiconductor device according to claim 74, wherein said semiconductor layer is a n-type GaN channel layer.

Claims 86 – 89 (Cancelled)